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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,830	11/15/2000	Toshiharu Furukawa	BUR9-2000-0029-US1	1095

7590 12/26/2002
IBM Corporation
Intellectual Property Law, 972E
1000 River Street
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EXAMINER

QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 12/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/713,830

Applicant(s)

FURUKAWA ET AL.

Examiner

Kevin Quinto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10 and 12-47 is/are pending in the application.
- 4a) Of the above claim(s) 22-43 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10, 12-21 and 44-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 10 and 12-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 45 is objected to because of the following informalities: the phrase "said lower portion of said gate extends beyond said lower portion to provide a T-shaped gate" is incorrect. The examiner believes that the intended phrase is *said upper portion of said gate extends beyond said lower portion to provide a T-shaped gate*. The examiner has interpreted the claim in this manner. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 10 and 12-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claim 20 (upon which claims 10, 12-19, and 21 depend) recites the limitation "said first material" in the fourth line of the claim as written in Exhibit A of the response filed October 9, 2002. There is insufficient antecedent basis for this limitation in the claim.

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6. The examiner has interpreted "said first material" to mean the first conductive material.

7. Claim 20 (upon which claims 10, 12-19, and 21 depend) contains the phrase "said first material has a dimension less than a photolithographic minimum dimension." The metes and bounds of this phrase are not clear to the examiner since the photolithographic minimum dimension changes as semiconductor device fabrication processes advance (from 180 nm to 130 nm to 90 nm).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 10, 12, 16, 19, 20, and 44-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (USPN 6,124,177).

10. So far as understood in claim 20, Lin et al. (USPN 6,124,177, hereinafter referred to as the "Lin" reference) discloses a similar device. Figure 8 of Lin illustrates a FET with a gate (22, 32) comprising a first conductive material (22) and a second conductive material (32). The second conductive material (32) is a silicide. This is different from the first conductive material (22) which is polysilicon. The second conductive material (32) extends beyond the first conductive material (22) to form a T-shaped gate. There is a first diffusion region (25) which is self-aligned to the first conductive material (22). There is a second diffusion region (24) which

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is defined by the second conductive material (32). There is a spacer (not labeled) which is along the sidewalls of the second conductive material (32). A third implant region (30) is defined by the spacer. The first conductive material (22) has a dimension less than a photolithographic minimum dimension (column 3, lines 34-39 and column 6, lines 35-39).

11. So far as understood in claim 10, the first conductive material (22) is on a gate dielectric (20). The gate dielectric (20) is on a substrate (10).

12. So far as understood in claims 12 and 16, the first conductive material (22) is polysilicon, thus comprising a first semiconductor material.

13. So far as understood in claim 19, the second conductive material (22) is a silicide.

14. In reference to claim 44, Lin discloses a similar device. Figure 8 illustrates FET with a gate (22, 32) disposed on a substrate (10). The gate (22, 32) has a lower portion (22) having first sidewalls and an upper portion (32) having second sidewalls. There are spacers (not labeled) disposed on the second sidewalls which extend down to the substrate (10) without contacting the first sidewalls to define an air gap (28).

15. With regard to claim 45, the upper portion (32) of the gate extends beyond the lower portion (22) thereby forming a T-shaped gate.

16. In reference to claim 46, there is a first implant region (25) in the substrate (10) which is aligned to the first sidewalls and a second implant region (24) which is aligned to the second sidewalls.

17. With regard to claim 47, there is a third implant (30) which is aligned to the spacers.

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Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,124,177) in view of Sagnes (USPN 5,998,289).

20. So far as understood in claim 13, Lin does not disclose the use of germanium as a material in the gate electrode. However the use of germanium as a gate electrode is well known in the art. Sagnes (USPN 5,998,289) discloses that using germanium in the gate electrode provides the benefit of compatibility with both n and p type transistors which leads to a more efficient fabrication process (column 1, lines 26-32). It would therefore be obvious to utilize germanium in the gate electrode of Lin in order to attain this benefit.

21. So far as understood in claim 21, figure 8 of Lin shows that there is an air gap (28) which is behind the spacer along a notched sidewall of the first conductive material (22).

22. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,124,177) in view of Naruse et al. (USPN 5,356,821).

23. So far as understood in claim 14, Lin does not disclose the use of a germanium compound ($\text{Ge}_x\text{Si}_{1-x}$ with $0.5 < x < 1.0$) as a material in the gate electrode. However the use of a germanium compound ($\text{Ge}_x\text{Si}_{1-x}$) as a gate electrode is well known in the art. Naruse et al. (USPN 5,356,821, hereinafter referred to as the "Naruse" reference) discloses that using a germanium compound ($\text{Si}_{1-x}\text{Ge}_x$) in the gate electrode provides the benefit of lower resistance

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(column 7, lines 18-29). Naruse discloses an example where $x = 0.52$ (column 7, lines 18-21); thus meeting the limitation where $0.5 < x < 1.0$. Naruse also discloses that as germanium content increases, the resistance decreases (column 7, lines 22-25). It would therefore be obvious to utilize a germanium compound ($\text{Ge}_x\text{Si}_{1-x}$ where $0.5 < x < 1.0$) in the gate electrode of Lin in order to attain the benefit of lower resistance.

24. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,124,177) in view of Price et al. (USPN 4,570,328).

25. So far as understood in claim 15, Lin does not disclose the use of polysilicon as the second conductive material in the gate electrode. However the use of polysilicon as material in a gate electrode is well known in the art. Price et al. (USPN 4,570,328, hereinafter referred to as the "Price" reference) discloses that using polysilicon in the gate electrode provides the benefit of compatibility with the high temperature processes which take place after the electrode and interconnect fabrication (column 1, lines 19-34). It would therefore be obvious to utilize polysilicon as the second conductive material in the gate electrode of Lin in order to attain this benefit.

26. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (USPN 6,124,177) in view of Rodder (USPN 6,087,248).

27. So far as understood in claims 17 and 18, Lin does not disclose the use of a refractory metal as the second conductive material in the gate electrode. However the use of a refractory metal as material in a gate electrode is well known in the art. Rodder (USPN 6,087,248) discloses that using a refractory metal such as tungsten in the gate electrode provides the benefit of being able to withstand the later high temperature processes (column 4, lines 32-38). It would

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therefore be obvious to utilize a refractory metal, such as tungsten, as the second conductive material in the gate electrode of Lin in order to attain this benefit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ

December 22, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

